WHAT IS CLAIMED IS:

1. A circuit comprising:

first and second field effect transistor devices arranged to provide parallel current paths between a supply voltage and an output node, the first and second transistor devices having oxide layers with a thickness of about 200 Angstroms or less; and

a component coupled to the output node that is intolerant of the supply voltage.

2. The circuit of claim 1 wherein the oxide layers have a thickness between about 100 Angstroms and about 190 Angstroms.

3. The circuit of claim 1 further comprising a current source coupled to the output node.

4. The circuit of claim 1 further comprising a third transistor device coupled to the output node and a circuit that activates the third transistor device when the first transistor device is deactivated.

5. The circuit of claim 1 further comprising switching logic to selectively activate the first transistor device.

6. The circuit of claim 1, wherein the transistor devices are selected from the group consisting of P devices and S devices.

7. The circuit of claim 6, wherein the first transistor device is a P device and the second transistor device is an S device.

8. The circuit of claim 7, wherein the S device is diode-connected to the voltage source.

9. The circuit of claim 1, wherein a third transistor device is disposed between the first transistor device and the output node and wherein the third transistor device has an oxide layer with a thickness greater than about 200 Angstroms.

10. The circuit of claim 1, wherein the supply voltage is selected from the group consisting of about 3 volts, about 5 volts and about 12 volts.

11. A computer system, comprising:

a central processor;

a system bus coupled to the processor;

a main memory coupled to said system bus; and

a programmable non-volatile long term memory coupled to said system bus, further comprising:

a flash EEPROM memory array; and

a circuit for providing a voltage substantially higher than Vcc to the EEPROM array, said circuit comprising:

first and second field effect transistor devices arranged to provide parallel current paths between a supply voltage and an output node, the first and second transistor devices having oxide layers with a thickness of about 200 Angstroms or less; and

a component coupled to the output node that is intolerant of the supply voltage.

12. The system of claim 11 wherein the oxide layers have a thickness of about 100 to about 190 Angstroms.

13. The system of claim 11 further comprising a current source coupled to the output node.

14. The system of claim 11 further comprising a third transistor device coupled to the output node and pull down switching logic that activates the transistor when the first transistor device is deactivated.

15. The system of claim 11 further comprising switching logic to selectively activate the first transistor device.

16. The system of claim 11, wherein the transistor devices are selected from the group consisting of P devices and S devices.

17. The system of claim 16, wherein the first transistor device is a P device and the second transistor device is an S device.

18. The system of claim 17, wherein the S device is diode-connected to the voltage source.

19. The system of claim 11, wherein a third transistor device is disposed between the first transistor device and the output node and wherein the third transistor device has an oxide layer with a thickness greater than about 200 Angstroms.

20. The system of claim 11, wherein the supply voltage is selected from the group consisting of about 3 volts, about 5 volts and about 12 volts.

21. A method comprising:

providing first and second field effect transistor devices arranged to provide parallel current paths between a supply voltage and an output node, the first and second transistor devices having oxide layers with a thickness of about 200 Angstroms or less, wherein the output node is coupled to a component that is intolerant of the supply voltage; and

selectively activating the first transistor device to pass substantially the entire supply to the output node.

22. The method of claim 21, further comprising bleeding sub-threshold current from the output node.

23. The method of claim 22, wherein the bleeding is performed by a current source coupled to the output node.

24. The method of claim 21, further comprising pulling down the output node voltage to the steady state output node voltage upon deactivation of the first transistor device.

25. The method of claim 24 wherein the pull down is effected by a third transistor device coupled to the output node and logic that activates the transistor when the first transistor device is deactivated.

26. The method of claim 21 wherein the oxide layers have a thickness of about 100 to about 190 Angstroms.

27. The method of claim 21 wherein the first transistor device is activated by a logic network.

28. The method of claim 21, wherein the transistor devices are selected from the group consisting of P devices and S devices.

29. The method of claim 28, wherein the first transistor device is a P device and the second transistor device is an S device.

30. The method of claim 29, wherein the S device is diode-connected to the voltage source.

31. The method of claim 21, wherein the supply voltage is selected from the group consisting of about 3 volts, about 5 volts and about 12 volts.